Single Event Upset Behavior of CMOS Static RAM cells

Kjell O. Jeppson*, Udo Lieneweg** and Martin G. Buehler**

Abstract

An improved state-space analysis of the CMOS static RAM cell is presented. Introducing the concept of the dividing line, the critical charge for heavy-ion-induced upset of memory cells can be calculated considering symmetrical as well as asymmetrical capacitive loads. From the critical charge, the upset-rate per bit-day for static RAMs can be estimated.

Introduction

To predict the heavy-ion-induced upset rate of static random access memory (SRAM) cells, Buehler and Allen [1] developed an analytical method based on state-space analysis [2]. Cell upsets are eventually caused if the hole-electron pairs generated along the track of an alpha particle hitting the memory cell, are, collected by the reverse-biased pn-junction of an output node. A 5-MeV alpha particle generates, roughly, one million hole-electron pairs corresponding to a charge of 0.16 pC. If this charge is collected by the reverse-biased pn-junction of an output node, this node is charged, or discharged. If the current pulse during the alpha hit is short compared to the response time of the cell, the node set and release approach [1] can be used. In this approach, the output node voltage is set by the alpha hit, whereafter the released cell is analyzed to see if the alpha hit causes an upset or not, For 5-MeV alpha particles, the node set and release approach is justified by the. fact that, even if the current pulse is best approximate by a decaying exponential with a time constant of 1 ns [3], most of the charges are collected within 200 ps [4],

Here, an improved analysis of the static RAM-cell in the release mode is presented which yields better understanding of the RAM-cell behavior and more accurate expressions of the critical upset charge. his analysis is based on cell behavior close to the meta-stable state rather than on empirical observations of the initial slopes of the node voltage curves.

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State-space analysis

The core of the CMOS static RAM cell is the bistable latch or flip-flop, which consists of two inverters as shown in Fig. 1. The two coupling nodes, N_1 and N_2, have effective capacitances to ground, C_1 and C_2, respectively, and a mutual capacitance C_m. The state of the flip-flop is described by the two

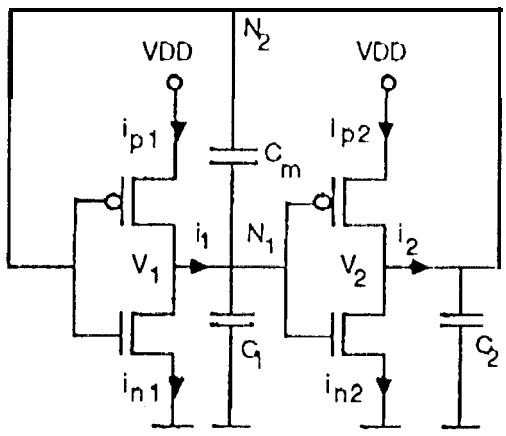

Fig. I. Two cross -coupled inverters are used to design a bistable flip-flop.

node voltages, V_1 and V_2. The bistable flip-flop has three steady states: the one-state (O, V_{DD}), the zero-state (V_{DD}, O) and the unstable state (V_{1M}, V_{2M}), ususally known as the metastable state.

The dynamic behaviour of the flip-flop is described by the current equations of the two nodes, i.e.:

$$C_1 \frac{dV_1}{dt} + C_m \left(\frac{dV_1}{dt} - \frac{dV_2}{dt} \right) = i_1 \qquad (1)$$

$$C_2 \frac{dV_2}{dt} + C_m \left(\frac{dV_2}{dt} - \frac{dV_1}{dt} \right) = i_2, \qquad (2)$$

where i_1 and i_2 are the currents flowing into the two nodes N_1 and N_2.

The two equations closing the system are governed by Kirchhoff's current law and gives

$$i_1 = i_{p1} - i_{n1} \quad (3)$$
$$i_2 = i_{p2} - i_{n2}, \quad (4)$$

where $i_{p1}(V_2, V_1)$ and $i_{p2}(V_1, V_2)$ are the currents through the two P-channel transistors and $i_{n1}(V_2, V_1)$ and $i_{n2}(V_1, V_2)$ are the currents through the two N-channel transistors, respectively.

The three steady state solutions of the system are given by

$$i_{p1} - i_{n1} = 0 \quad (5)$$
$$i_{p2} - i_{n2} = O, \quad (6)$$

where the two equations represent the transfer curves of the two inverters, as shown in Fig, 2.

If the flip-flop, for any reason such as an alpha particle hit, is upset from its steady states, the "return-trajectory" from any given state, (V_{10}, V_{20}), to one of the steady states has to be derived numerically. This is because of the complicated non-linear voltage dependence of the transistor and capacitor models, which results in non-linear differential equations, and which generally cannot be solved analytically. The most convenient way to solve the problem is to use a circuit simulator such as SPICE. A typical example of such simulations is shown in Fig. 3.

Equations (1) and (2) give directly the velocity in state space

$$\left(\frac{dV_1}{dt}, \frac{dV_2}{dt}\right)$$

if the dc current-voltage characteristic of the latch, $(i_1(V_2,V_1), i_2(V_1,V_2))$, and the node capacitances are known. Fig, 4 shows the two velocity components, and Fig. 5 gives a vector field representation. As illustrated in Fig. 4, each velocity component is zero along the corresponding transfer curve (as long as the mutual capacitance can be neglected). For the steady state solutions both velocity components are zero. From the velocity vector field the slope, dV_2/dV_1, is known analytically in any point along each of the return trajectories in Fig. 3. The velocity vector field also allows a crude graphical construction of the return trajectories by following the directions given by the vectors as illustrated in Fig. 5. Note that the return trajectories will always cross the static transfer curve characterized by i2=0 horizontally, and the other static transfer curve (i_1=0) vertically [5].

Of particular interest with respect to single event upsets, are the two trajectories leading to the metastable point. These two trajectories divide the state-plane into two halves and will serve as a "separatrix" [6] or "dividing line" during the alpha particle hit. If this dividing line is crossed during the hit, the cell will be upset and change its state during the following "release" mode, otherwise it will return to the same state as before. The next section will give an analytical expression for the dividing line as a guide for the RAM designer.

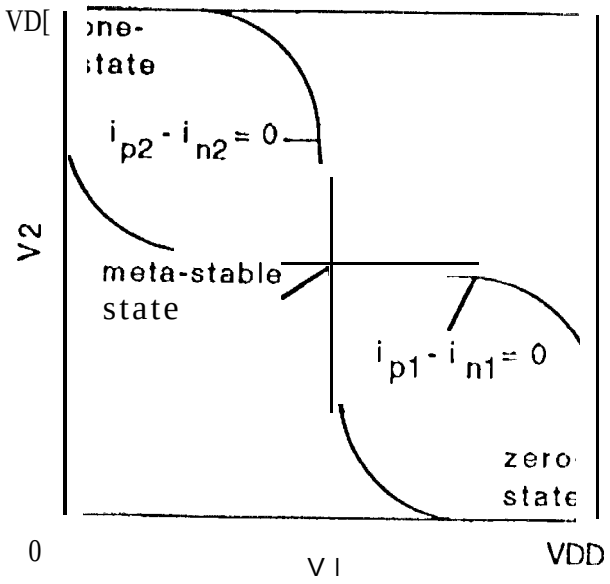

Fig. 2. The static transfer curves of the two inverters in a flip-flop are illustrated in the (VI, V_2) state plane.

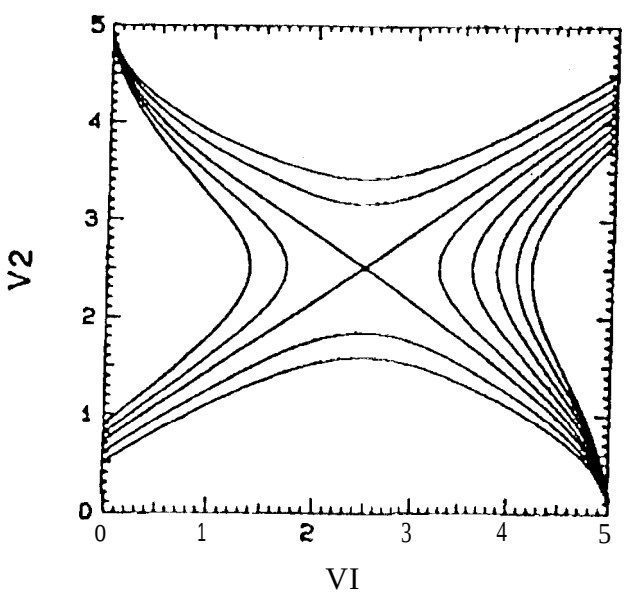

Fig. 3. SPICE-simulated "return-trajectories" to one of the stable states from an arbitrary point (V_{10}, V_{20}), in the (VI, V_2) state plane.

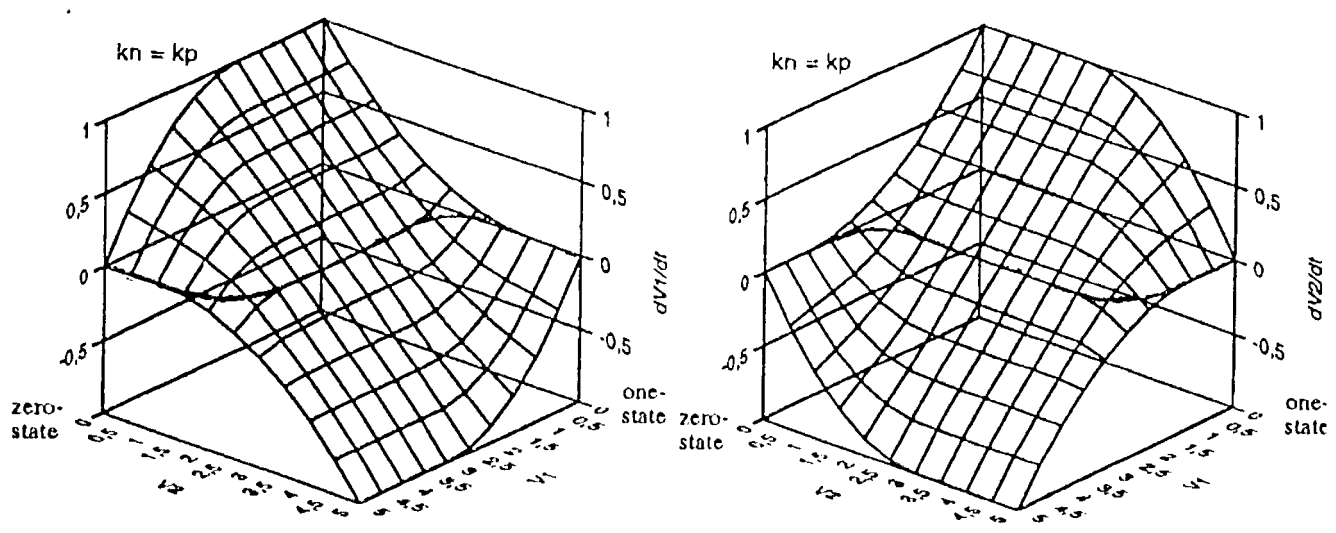

Fig. 4. *Phase-space diagrams for the velocities dV_1/dt and dV_2/dt.*

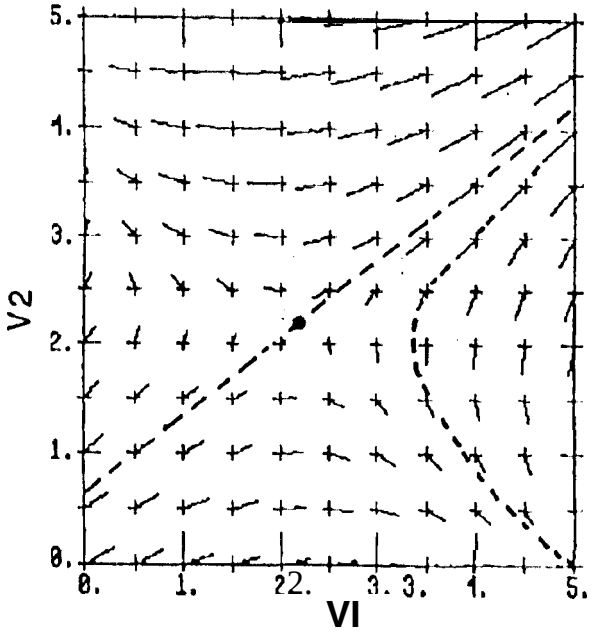

Fig. 5. The velocity vector field in the (V_1, V_2) state plane for C_1/C_2=0.5 and β_n/β_n=3.3. Also shown cre a return trajectory and the separatrices ending in the metastable point.

Analytical Description of Dividing Line

To derive analytical expressions for the dividing line, simplified transistor models must be used. Simulations using different transistor models suggest that the trajectories leading to the metastable state, i.e. the dividing line, with very good accuracy can be approximated by a straight line. To derive an expression for the slope of this line, transistor currents i_1 and i_2 are linearized around the metastable point. Assuming identical inverters (except for the capacitive loads), and neglecting the mutual capacitance C_m and the output conductances of the transistors, we obtain from Eqs (1) and (2),

$$\frac{dV_2}{dV_1} = \frac{C_1}{C_2} \frac{(g_{mn} + g_{mp})(V_1 - V_M)}{(g_{mn} + g_{mp})(V_2 - V_M)}, \qquad (7)$$

where g_{mn} and g_{mp} are the transconductances in the metastable point (V_M, V_M) of (he n- and p-channel transistors, respectively. Assuming a linear relationship between V_2 and VI along the dividing line,

$$V_2 - V_M = K (V_1 - V_M), \qquad (8)$$

where $K = dV_2/dV_1$, wc obtain

$$K = \pm \sqrt{\frac{C_1}{C_2}}. \qquad (9)$$

This result suggests that the RAM cell enters the metastable state along a straight line with slope $\sqrt{C_1/C_2}$, and leaves it along another straight line with slope $-\sqrt{C_1/C_2}$. The dividing line is therefore given by

$$V_2 - V_M = \sqrt{\frac{C_1}{C_2}} (V_1 - V_M). \qquad (10)$$

Simulations show that this equation for the dividing line is a very good approximation of the simulated behavior. To examine closer the justification of assuming a constant

transconductance in the saturation region, let us use a modified Shockley transistor model giving the saturation current as

$$i_n = k_n \frac{(V_{GS}-V_{TN})^2}{2(1+\delta_n)}, \qquad (11)$$

where k_n is the transistor gain factor, V_{TN} the threshold voltage and δ_n the Taylor series expansion coefficient of the bulk charge, (In standard textbook equations, usually $\delta_n=0$.) The transistor is saturated for $V_{DS} \geq V_{DSAT} = (V_{GS}-V_{TN})/(1+\delta_n)$. The linear region drain current is given by

$$i_n = k_n\left[(V_{GS}-V_{TN})V_{DS} - (1+\delta_n)\frac{V_{DS}^2}{2}\right] \qquad (12)$$

Using similar equations for the p-channel transistor, we can write the two node currents as

$$i_1(V_2) = \frac{\beta_p}{2}(V_2-V_{DD}-V_{TP})^2 - \frac{\beta_n}{2}(V_2-V_{TN})^2 \qquad (13)$$

and

$$i_2(V_1) = \frac{\beta_p}{2}(V_1-V_{DD}-V_{TP})^2 - \frac{\beta_n}{2}(V_1-V_{TN})^2, \qquad (14)$$

where for a q-type transistor $\beta_q = \frac{k_q}{1+\delta_q}$.

For the case of $\beta_n = \beta_p = \beta$, we obtain a constant transconductance,

$$g_m = g_{mn} + g_{mp} = -\beta\,(V_{DD} + V_{TP} - V_{TN}), \qquad (15)$$

for the whole region[1] where all four transistors are saturated. Hence, for this region (shown shaded in Fig. 6) the linear equation given by Eq. (10) is an exact solution for the dividing line

For the general case when $\beta_n \neq \beta_p$, we obtain from Eqs (1) and (2) neglecting C_m

$$\frac{dV_2}{dV_1} = \frac{C_1}{C_2}\frac{i_2(V_1)}{i_1(V_2)}. \qquad (16)$$

Separating variables, we obtain after integration

$$C_1\left[\beta_p(V_{DD}+V_{TP}-V_1)^3 + \beta_n(V_1-V_{TN})^3 - \beta_p(V_{DD}+V_{TP}-V_M)^3 - \beta_n(V_M-V_{TN})^3\right] = C_2\left[\beta_p(V_{DD}+V_{TP}-V_2)^3 + \beta_n(V_2-V_{TN})^3 - \beta_p(V_{DD}+V_{TP}-V_M)^3 - \beta_n(V_M-V_{TN})^3\right], \qquad (17)$$

where the metastable point (V_M, V_M) is given by

$$V_M = \frac{V_{DD}+V_{TP}+\sqrt{\frac{\beta_n}{\beta_p}}\,V_{TN}}{1+\sqrt{\frac{\beta_n}{\beta_p}}} \qquad (18)$$

Eq. (17) is valid when all four transistors are saturated. It can also be made valid for turned-off transistors, if the negative value of the corresponding parenthesis is replaced by zero.

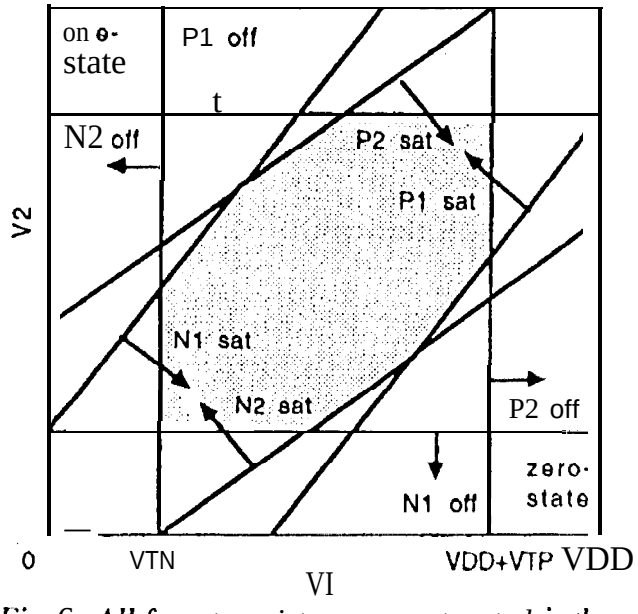

Fig. 6. All four transistors are saturated in the shadowed area. $\delta_n = \delta_p = 0.3$, $V_{TN} = -V_{TP} = 1$ V.

[1] This region is given by

$$\frac{V_1-V_{TN}}{1+\delta_n} \leq V_2 \leq V_{DD} + \frac{V_1-V_{DD}-V_{TP}}{1+\delta_p}$$
$$\frac{V_2-V_{TN}}{1+\delta_n} \leq V_1 \leq V_{DD} + \frac{V_2-V_{DD}-V_{TP}}{1+\delta_p}$$
$$V_{TN} \leq V_1 \leq V_{DD} - V_{TP}$$
$$V_{TN} \leq V_2 \leq V_{DD} - V_{TP}$$

The previously obtained straight line solution for the case of $\beta_n=\beta_p$, given in Eq. (10), is simply a special case[2] of the general solution.

A plot of the dividing line for the case of β_n/β_p = 3.3 is shown in Fig. 7 using C_1/C_2 = 1, 0.7, 0.5, 0.25 and 0.1 as parameter values. As indicated by Fig. 7, the dividing line is very close to a straight line also for $\beta_n \neq \beta_p$[3]. As an example, the second order deviation in V_2 for $V_1=V_{DD}$ is less than 5% for $\beta_n/\beta_p=3.3$ and $C_1/C_2 \geq 0.1$.

Comparisons to SPICE simulations show that the solution of Eq. (17) can be extended with small errors also into regions of the state-plane where one transistor is linear. if the current through this transistor is small compared to the current through the other transistor of the same inverter. For the example of Fig. 7, where β_n/β_p = 3.3, transistor PI becomes linear along the dividing line when $C_1/C_2 \leq 0.39$. However, the error is negligible as long as i_{p1} is less than one tenth of i_{n1} (which is true for $C_1/C_2 \geq 0.07$).

For the limiting case of very small C_1/C_2 capacitance ratios, the dividing line becomes a horizontal line through the metastable state. The return track from the metastable state to one of the stable states coincides with the static transfer curve (i_1=0). For very large C_1/C_2 capacitance ratios the limiting dividing line is a vertical line through the metastable state. The return track from the metastable state to one of the stable states now coincides with the other static transfer curve (i_2=0). See Appendix,

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[2] For $\beta_n=\beta_p$, Eq. (17) yields

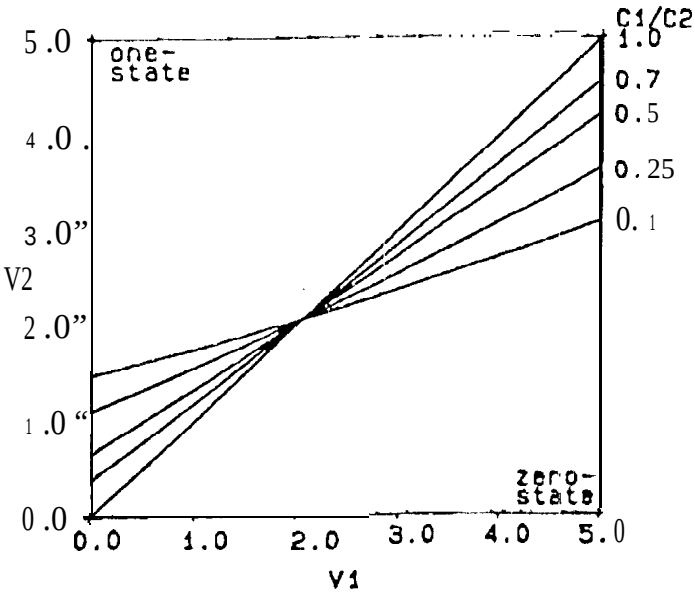
$$C_2(V_{DD}+V_{TP}-V_{TN})(V_2-V_M)^2 = C_1(V_{DD}+V_{TP}-V_{TN})(V_1-V_M)^2,$$

from which Eq. (10) can be obtained. For that part of the dividing line that falls outside the shaded region where all four transistors are saturated, for instance when P2 is turned off (for $C_1/C_2<1$), Eq. (22) yields

$$C_1[(v_1-V_{TN})^3-(V_{DD}+V_{TP}-V_M)^3-(V_M-V_{TN})^3] = 3C_2(V_{DD}+V_{TP}-V_{TN})(V_2-V_M)^2,$$

which only slightly deviates from a straight line.

[3] It is exactly a straight line for $C_1=C_2$.



Fig, 7. The dividing line with C_1/C_2 = 1, 0.7, 0.5, 0.25 *and 0.1 as parameter.*

Critical Charge Expressions

To calculate the upset-rate of a static RAM in space, Buehler and Allen used the Petersen equation [7] which assumes a 10-percent worst case differential cosmic-ray spectrum. According to the Petersen equation, the upset rate (in upsets per bit-day) for a heavy-ion hit on a q-type reverse-biased pn-junction of node i is given by

$$R_i = 5.10^{-10} AJ_{qi}\left(\frac{X_q}{QC_{qi}}\right)^2 \qquad (19)$$

where AJ_{qi} is the area of the reverse-biased pn-junction of node i (in μm^2), X_{qi} is the carrier collection depth of the same junction (in μm) and QC_{qi} is the critical charge (in pC).

The critical charge for a heavy-ion-induced upset can be calculated for each reverse-biased pn-junction of the RAM cell using the results from the previous analysis.

For $C_1/C_2<1$, the critical charges for a hit of inverter 2 is calculated as follows. With the RAM cell being in the zero-state, V_2=0 and the drain of transistor P2 is reverse-biased. The critical voltage, VC_{p2}, for a P2 heavy-ion hit is obtained from the dividing line at $V_1=V_{DD}$ [1]. In the one-state, $V_2=V_{DD}$ and the drain of transistor N2 is reverse-biased. The critical

voltage, VC_{n2}, for an N2 heavy-ion hit is obtained from the dividing line at V_1==O [1].

Therefore, the critical voltages can be obtained from the straight line equation (10) as

$$VC_{p2} = V_M + \sqrt{\frac{C_1}{C_2}}(V_{DD} - V_M) \qquad (20)$$

and

$$VC_{n2} = V_M\sqrt{\frac{C_1}{C_2}}V_M, \qquad (21)$$

respectivel y.

The expression for VC_p2 of Eq. (20) can be compared to the expression derived by Buehler and Allen. They based their analysis on the empirical observation that

$$\frac{dV_2}{dV_1} = \frac{VC_{p2}}{V_{DD}} \qquad (22)$$

at (V_{DD}, VC_{p2}) in the state-plane. After some approximations their derivation yielded

$$VC_{p2} = V_{TN} + \sqrt{\frac{C_1}{C_2}}(V_{DD} - V_{TN}). \qquad (23)$$

Here, it can be seen that while their expression for VC_{p2} only depends on the threshold voltage of the n-channel transistors, the new expression in Eq. (20) depends on the switching voltage of the inverter. Thereby, the influence of both the p- and n-channel transistors are considered,

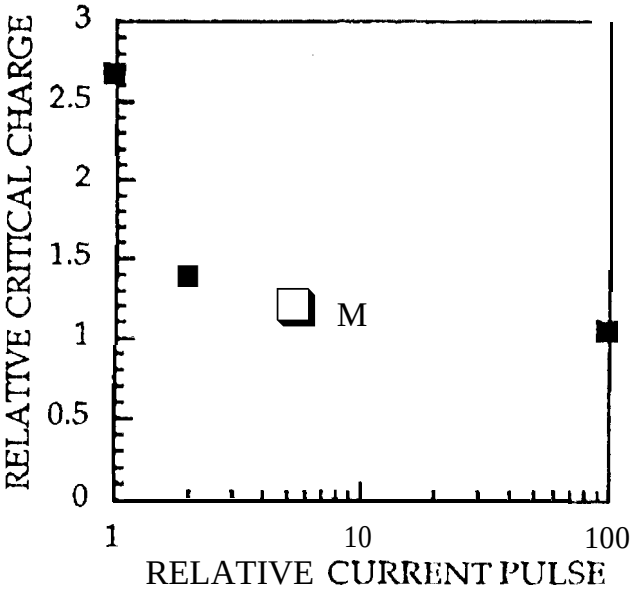


Fig. 8. The relative critical charge for memory upset versus the relative current pulse (normalized to the transistor saturation current).

From the critical voltages, VC_{p2} and VC_{n2}, Buehler and Allen [1] defined the corresponding critical charges for memory upset by a P2- and N2-hit as

$$QC_{p2} = C_2\, VC_{p2} \qquad (24)$$

and

$$QC_{n2} = C_2\,(V_{DD} - VC_{n2}), \qquad (25)$$

respectively.

The critical charge is the minimum charge needed for memory upset, assuming that the charge is collected so rapidly that the voltage on the other node does not change. This is true for most memory cells since they, typically, have a slow response time (>500 ps) and most of the charge is collected within 200 ps as shown by [4]. However, if charge is lost during the alpha hit and, more charge must be collected to upset the cell, To simulate the cell during the alpha hit, one must be concerned with the detailed nature of the current pulse. For 5 MeV alpha particles, the current pulse can be approximated by a decaying exponential with a time constant of 1 ns [3]. However, in most cases, as the simulated cases shown in Fig. 8, a simple square-wave current pulse is a good enough first-order approximation [8]. The corresponding set and release trajectories simulated for five different current sources are shown in Fig. 9.

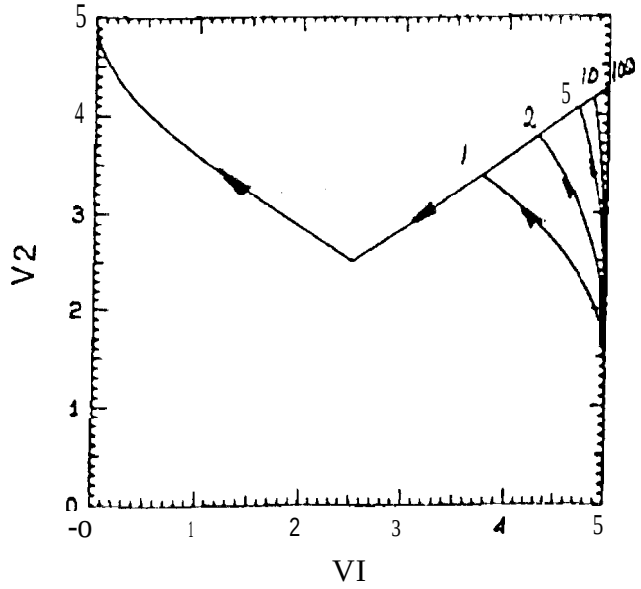


Fig. 9. The set and release trajectories for five different current pulses during the alpha hit. The cur-rent pulse is normalized to the transistor saturation current.

The critical charges for a hit of inverter 1 can be calculated similarly, at least for capacitively symmetric RAM cells or when $C_1/C_2>1$. In order to estimate the critical charges for N1 or P1 hits when $C_1/C_2<1$, one has to know how the dividing line continues into the regions where $V_1<0$ and $V_1>V_{DD}$. Due to the forward biasing of the drain diodes N1 or P1, respectively, large restoring currents i_r develop, bending the dividing line almost horizontal outside the frame of Fig. 7. Consequently, the dividing line will be impossible to reach by N 1 or P 1 hits, i. e. QC_{N1} and QC_{P1} become very large and the corresponding upset rates can be neglected.

Conclusions

A dynamic description of the charging and discharging behavior of bistable RAM cells after single event upsets has been developed, State plane analysis has been shown 'to be a useful tool in providing insight into basic RAM cell behavior, both in the set mode during alpha particle hit and in the release mode after the hit, The state plane has been shown to be divided into two halves by a dividing line that determines to which stable state the system returns after a hit. Analytic expressions for the dividing line, and for the minimum critical upset charges, have been given.

Acknowledgements

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References

1. M. Buehler and R. Allen, "An Analytical Method for Predicting CMOS SRAM Upsets with Application to Asymmetrical Memory Cells", *IEEE Transaction on Nuclear Science,* NS-33, pp 1637-1641 (1986)
2. R. C. Jaeger and R. M. Fox, "Analytic Expressions for the Critical Charge in CMOS Static RAM Cells", *IEEE Transactions on Nuclear Science,* NS-30, *4616-4619* (1983)
3. R. J. McPartland, "Circuit Simulations of Alpha-Particle-Induced Soft Errors in MOS Dynamic RAM 's", *IEEE Journal of Solid-State Circuits, SC- 16,31-34 (1981)*
4. C. M. Hsieh, P. C. Murley and R. R. O'Brien, "Dynamics of Charge Collection from Alpha-Particle Tracks in Integrated Circuits", in *Proceedings of 10th Annual International Reliability Symposium.* Orlando, FL, 38-42 (1981)
5. L. A. Glasser and D. W. Dobberpuhl, *The Design and Analysis of VLSI Circuits,* Chap 5 (Fig.5.38), Reading, MA, USA: Addison-Wesley, (1985)
6. D. K. Arrowsmith and C. M. Place, *Ordinary Differential Equations,* London, New York: Chapman and Hall (1982)
7. E. L. Petersen, J. B. Langworthy and S. E. Diehl, "Suggested Single Event Upset Figure of Merit", *IEEE Transaction on Nuclear Science,* NS-30, pp 4533-4539 (1983)
8. Y. Idei, N. Homma, H. Nambu and Y. Sakurai, "Soft-Error Characteristics in Bipolar Memory Cells with Small Critical Charge", *IEEE Transactions on Electron Devices, ED-38, 2465-2471* (1991)

Appendix

Generally, Eqs (1) and (2) can he rewritten as

$$\frac{dV_1}{dt} = \frac{i_1}{C_{11}} + \frac{i_2}{C_{12}} \qquad \text{(A1)}$$

$$\frac{dV_2}{dt} = \frac{i_1}{C_{21}} + \frac{i_2}{C_{22}}, \qquad \text{(A2)}$$

where

$$C_{11} = C_1 + \frac{c_m}{1 + \frac{C_m}{C_2}} \qquad \text{(A3)}$$

$$C_{12} = C_2 \frac{C^*_1}{C_m} + C_1 + C_2 \qquad \text{(A4)}$$

$$C_{21} = C_1 \frac{C_2}{C_m} + C_1 + C_2 \qquad \text{(As)}$$

$$C_{22} = C_2 + \frac{C_m}{1 + \frac{C_m}{C_1}} \qquad \text{(A6)}$$

Using the following linear approximation of the transistor currents,

$$i_1 = g_m (V_2 - V_M) + g_o (V_1 - V_M) \qquad \text{(A7)}$$

$$i_2 = g_m (V_1 - V_M) + g_o (V_2 - V_M), \qquad \text{(A8)}$$

where $g_m = g_{mn} + g_{mp}$ is the sum of the n- and p-channel transconductances in the metastable point (V_M, V_M) and $g_o = g_{on} + g_{op}$ is the sum of the output conductance, we obtain

$$\frac{dV_2}{dV_1} = \frac{a_2(V_2 - V_M) + b_2(V_1 - V_M)}{a_1(V_2 - V_M) + b_1(V_1 - V_M)}. \qquad (*9)$$

Here

$$a_1 = \frac{g_m}{C_{11}} + \frac{g_o}{C_{12}}, \qquad a_2 = \frac{g_m}{C_{21}} + \frac{g_o}{C_{22}}, \qquad \text{(A10)}$$

$$b_1 = -\frac{g_m}{C_{12}}, \qquad b_2 = \frac{g_o}{C_{21}} + \frac{g_m}{C_{22}}. \qquad \text{(A11)}$$

Assuming a linear relationship between V_2 and VI along the dividing line, i. c.

$$V_2 - V_M = K (V_1 - V_M), \qquad \text{(A12)}$$

we obtain the slope

$$K = -\frac{1}{2}\left(\frac{b_1}{a_1} - \frac{a_2}{a_1}\right) \pm \sqrt{\frac{1}{4}\left(\frac{b_1}{a_1} - \frac{a_2}{a_1}\right)^2 + \frac{b_2}{a_1}}. \qquad \text{(A13)}$$

If the mutual capacitance can be neglected compared to the load capacitances, [he expression for the slope reduces to

$$K = \pm\sqrt{\frac{C_1}{C_2} + c^2} - c \qquad \text{(A14)}$$

where

$$c = \frac{1}{2}\frac{g_o}{g_m}\left(1 - \frac{C_1}{C_2}\right).$$

As expected, this expression reduces further to $K = \pm\sqrt{\frac{C_1}{C_2}}$ hen assuming $g_o = 0$. Assuming $g_o \neq 0$ and letting $C_2 \to \infty$, we obtain from Eq. (A14)

$$K = \begin{cases} 0 \\ -\frac{g_o}{g_m}, \end{cases} \qquad \text{(A15)}$$

which confirms an incoming horizontal line to the metastable state and an outgoing line with a slope given by the reciprocal gain of the inverter. Letting $C_1 \to \infty$, we obtain

$$K = \begin{cases} \infty \\ -\frac{g_m}{g_o}, \end{cases} \qquad \text{(A16)}$$

which confirms an incoming vertical line to the metastable state and an outgoing line with a slope given by the gain of the inverter.

Finally, if the mutual capacitance cannot be neglected, we obtain assuming $g_o = 0$

$$K = \pm\sqrt{\frac{C_{11}}{C_{22}}} \qquad \text{(A17)}$$

Single Event Upset Behavior of CMOS Static RAM cells

Kjell O. Jeppson*, Udo Lieneweg** and Martin G. Buehler**

Abstract

An improved state-space analysis of the CMOS static RAM cell is presented. Introducing the concept of the dividing line, the critical charge for heavy-ion-induced upset of memory cells scan be calculated considering symmetrical as well as asymmetrical capacitive loads. From the critical charge, the upset-rate per bit-day for static RAMs can be estimated.

Introduction

To predict the heavy-ion-induced upset rate of static random access memory (SRAM) cells, Buehler and Allen [1] developed an analytical method based on state-space analysis [2]. Cell upsets are eventually caused if the hole-electron pairs generated along the track of an alpha particle hitting the memory cell, are collected by the mwerse-biased pn-junction of an output node. A 5-MeV alpha particle generates, roughly, onc million hole-electron pairs corresponding to a charge of 0.16 pC. If this charge is collected by the reverse-biased pn-junction of an output node, this node is charged, or discharged. If the current pulse during the alpha hit is short compared to the response time of the cell, the node set and release approach [1] can be used. In this approach, the output node voltage is set by the alpha hit, whereafter the released cell is analyzed to see if the alpha hit causes an upset or not. For 5-MeV alpha particles, the node set and release approach is justified by the fact that, even if the current pulse is best approximate by a decaying exponential with a time constant of 1 ns [3], most of the charges are collected within 200 ps [4].

Here, an improved analysis of the static RAM-ceil in the release mode is presented which yields better understanding of the RAM-cell behavior and more accurate expressions of the critical upset charge. This analysis is based on cell behavior close to the recta-stable state rather than on empirical observations of the initial slopes of the node voltage curves.

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State-space analysis

The core of the CMOS static RAM cell is the bistable latch or flip-flop, which consists of two inverters as shown in Fig. 1. The two coupling nodes, N_1 and N2, have effective capacitances to ground, C_1 and C_2, respectively, and a mutual capacitance C_m. The state of the flip-flop is described by the two

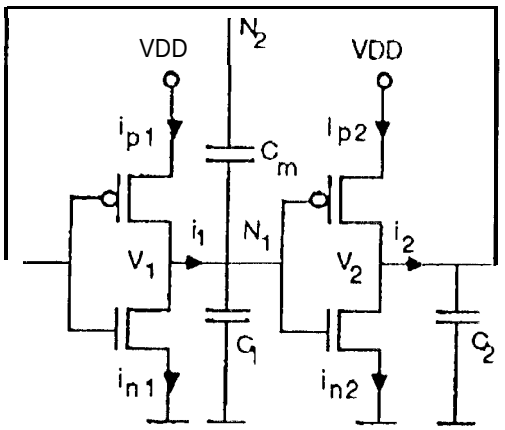

Fig. 1. Two cross-coupled inverters are used to design a bistable flip-flop.

node voltages, V_1 and V_2. The bistable flip-flop has three steady states: the one-state (O, V_{DD}), the zero-state (V_{DD}, O) and the unstable state (V_{1M}, V_{2M}), ususally known as the metastable state.

The dynamic behaviour of the flip-flop is described by the current equations of the two nodes, i.e.:

$$C_1 \frac{dV_1}{dt} + C_m \left(\frac{dV_1}{dt} - \frac{dV_2}{dt} \right) = i_1 \qquad (1)$$

$$C_2 \frac{dV_2}{dt} + C_m \left(\frac{dV_2}{dt} - \frac{dV_1}{dt} \right) = i_2, \qquad (2)$$

where i_1 and i_2 are the currents flowing into the two nodes N_1 and N_2.

The two equations closing the system are governed by Kirchhoff's current law and gives

$$i_1 = i_{p1} - i_{n1} \quad (3)$$
$$i_2 = i_{p2} - i_{n2}, \quad (4)$$

where $i_{p1}(V_2, V_1)$ and $i_{p2}(V_1, V_2)$ are the currents through the two P-channel transistors and $i_{n1}(V_2, V_1)$ and i_{n2} (Vi, V_2) are the currents through the two N-channel transistors, respectively.

The three steady state solutions of the system are given by

$$i_{p1} - i_{n1} = 0 \quad (5)$$
$$i_{p2} - i_{n2} = O, \quad (6)$$

where the two equations represent the transfer curves of the two inverters, as shown in Fig. 2.

If the flip-flop, for any reason such as an alpha particle hit, is upset from its steady states, the "return-trajectory" from any given state, (V_{10}, V_{20}), to one of the steady states has to be derived numerically. This is because of the complicated non-linear voltage dependence of the transistor and capacitor models, which results in non-linear differential equations, and which generally cannot be solved analytically. The most convenient way to solve the problem is to usc a circuit simulator such as SPICE. A typical example of such simulations is shown in Fig, 3.

Equations (1) and (2) give directly the velocity in state space

$$\left(\frac{dV_1}{dt}, \frac{dV_2}{dt}\right)$$

if the dc current-voltage characteristics of the latch, $(i_1(V_2,V_1), i_2(V_1,V_2))$, and the node capacitances are known. Fig. 4 shows the two velocity components, and Fig, 5 gives a vector field representation. As illustrated in Fig. 4, each velocity component is zero along the corresponding transfer curve (as long as the mutual capacitance can be neglected). For the steady state solutions both velocity components are zero. From the velocity vector field,.the slope, dV_2/dV_1, is known analytically in any point along each of the return trajectories in Fig. 3, The velocity vector field also allows a crude graphical construction of the return trajectories by following the directions given by the vectors as illustrated in Fig. 5. Note that the return trajectories will always cross the static transfer curve characterized by i2=0 horizontally, and the other static transfer curve (i_1=0) vertically [5].

Of particular interest with respect to single event upsets, arc the two trajectories leading to the metastable point, These two trajectories divide the state-plane into two halves and will serve as a "separatrix" [6] or "dividing line" during the alpha particle hit. If this dividing line is crossed during the hit, the cell will be upset and change its state during the following "release" mode, otherwise it will return to the same state as before. The next section will give an analytical expression for the dividing line as a guide. for the RAM designer.

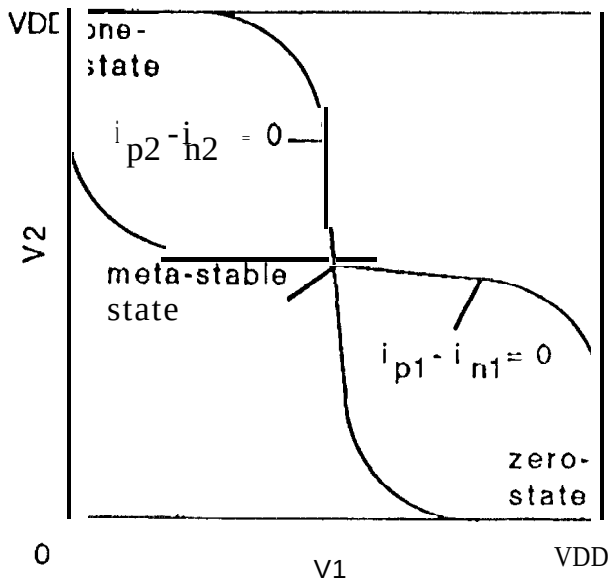

Fig. 2. The static transfer curves of the two inverters in a flip-flop are illustrated in the (V], V_2) state plane.

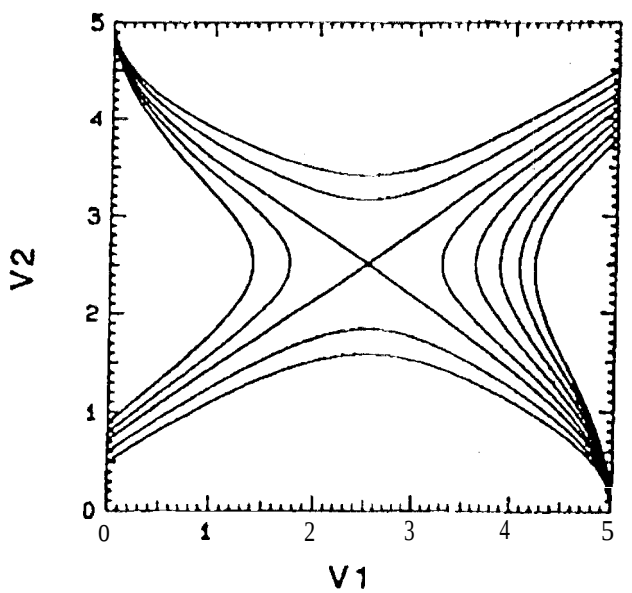

Fig. 3. SPICE-simulated "return-trajectories" to one of the stable states from an arbitrary point (V_{10}, V_{20}), in the (VI, V_2) state plane.

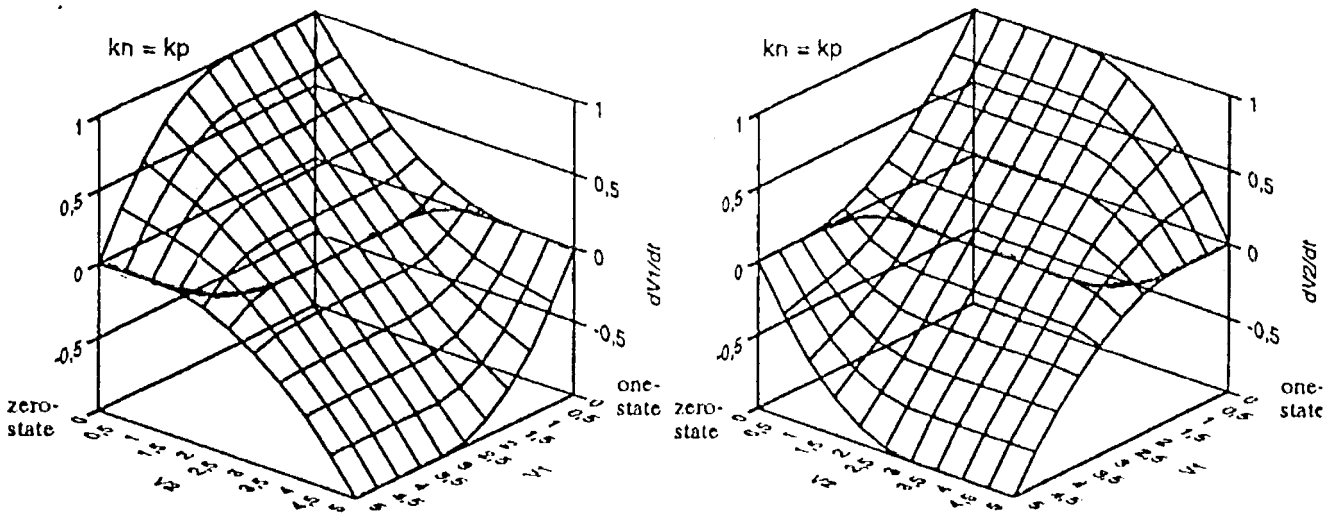

Fig. 4. *Phase-space diagrams for the velocities dV_1/dt and dV_2/dt.*

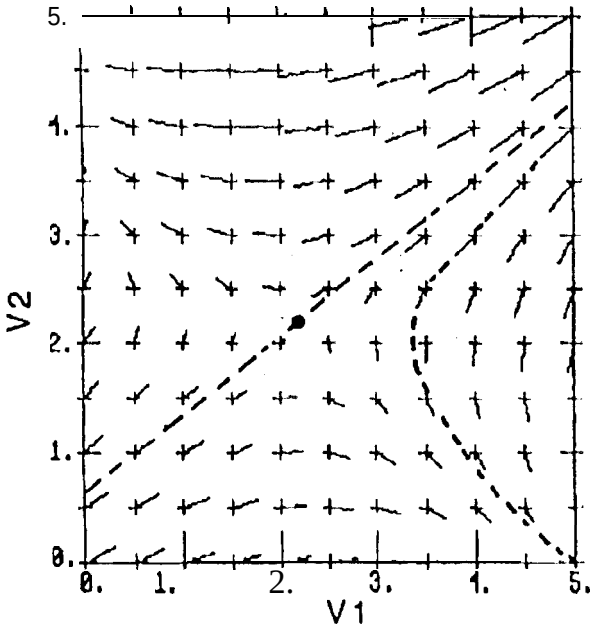

Fig. 5. The *velocity vector field in the (V_1, V_2) state plane for C_1/C_2=0.5 and β_n/β_n=3.3. Also shown cre a return trajectory and the separatrices ending in the metastable point.*

Analytical Description of Dividing Line

To derive analytical expressions for the dividing line, simplified transistor models must be used. Simulations using different transistor models suggest that the trajectories leading to the metastable state, i.e. the dividing line, with very good accuracy can be approximated by a straight line. To derive an expression for the slope of this line, transistor currents i_1 and i_2, are linearized around the metastable point. Assuming identical inverters (except for the capacitive loads), and neglecting the mutual capacitance C_m and the output conductance of the transistors, we obtain from Eqs (1) and (2),

$$\frac{dV_2}{dV_1} = \frac{C_1}{C_2} \frac{(g_{mn} + g_{mp})(V_1 - V_M)}{(g_{mn} + g_{mp})(V_2 - V_M)}, \qquad (7)$$

where g_{mn} and g_{mp} are the transconductances in the metastable point (V_M, V_M) of the n- and p-channel transistors, respectively. Assuming a linear relationship between V_2 and V_1 along the dividing line,

$$V_2 - V_M = K (V_1 - V_M), \qquad (8)$$

where $K = dV_2/dV_1$, we obtain

$$K = \pm \sqrt{\frac{C_1}{C_2}}. \qquad (9)$$

This result suggests that the RAM cell enters the metastable state along a straight line with slope $\sqrt{C_1/C_2}$, and leaves it along another straight line with slope $-\sqrt{C_1/C_2}$. The dividing line is therefore given by

$$V_2 - V_M = \sqrt{\frac{C_1}{C_2}} (V_1 - V_M). \qquad (10)$$

Simulations show that this equation for the dividing line is a very good approximation of the simulated behavior. To examine closer the justification of assuming a constant

transconductance in the saturation region, let us use a modified Shockley transistor model giving the saturation current as

$$i_n = k_n \frac{(V_{GS}-V_{TN})^2}{2(1+\delta_n)}, \qquad (11)$$

where k_n is the transistor gain factor, V_{TN} the threshold voltage and δ_n the Taylor series expansion coefficient of the bulk charge, (In standard textbook equations, usually $\delta_n=0$.) The transistor is saturated for $V_{DS} \geq V_{DSAT} = (V_{GS}-V_{TN})/(1+\delta_n)$. The linear region drain current is given by

$$i_n = k_n\left[(V_{GS}-V_{TN})V_{DS} - (1+\delta_n)\frac{V_{DS}^2}{2}\right] \qquad (12)$$

Using similar equations for the p-channel transistor, we can write the two node currents as

$$i_1(V_2) = \frac{\beta_p}{2}(V_2-V_{DD}-V_{TP})^2 - \frac{\beta_n}{2}(V_2-V_{TN})^2 \qquad (13)$$

and

$$i_2(V_1) = -\frac{\beta_p}{2}(V_1-V_{DD}-V_{TP})^2 - \frac{\beta_n}{2}(V_1-V_{TN})^2, \qquad (14)$$

where for a q-type transistor $\beta_q = \frac{k_q}{1+\delta_q}$.

For the case of $\beta_n = \beta_p = \beta$, we obtain a constant transconductance,

$$g_m = g_{mn} + g_{mp} = -\beta\left(V_{DD} + V_{TP} - V_{TN}\right), \qquad (15)$$

for the whole region[1] where all four transistors are saturated. Hence, for this region (shown shaded in Fig. 6) the linear equation given by Eq. (10) is an exact solution for the dividing line

For the general case when $\beta_n \neq \beta_p$, we obtain from Eqs (1) and (2) neglecting C_m

$$\frac{d\,V_2}{dV_1} = \frac{C_1}{C_2}\frac{i_2(V_1)}{i_1(V_2)}. \qquad (16)$$

Separating variables, we obtain after integration

$$C_1\left[\beta_p(V_{DD}+V_{TP}-V_1)^3 + \beta_n(V_1-V_{TN})^3 - \beta_p(V_{DD}+V_{TP}-V_M)^3 - \beta_n(V_M-V_{TN})^3\right] =$$
$$C_2\left[\beta_p(V_{DD}+V_{TP}-V_2)^3 + \beta_n(V_2-V_{TN})^3 - \beta_p(V_{DD}+V_{TP}-V_M)^3 - \beta_n(V_M-V_{TN})^3\right], \qquad (17)$$

where the metastable point (V_M, V_M) is given by

$$V_M = \frac{V_{DD}+V_{TP}+\sqrt{\frac{\beta_n}{\beta_p}}\,V_{TN}}{1+\sqrt{\frac{\beta_n}{\beta_p}}} \qquad (18)$$

Eq. (17) is valid when all four transistors are saturated. It can also be made valid for turned-off transistors, if the negative value of the corresponding parenthesis is replaced by zero.

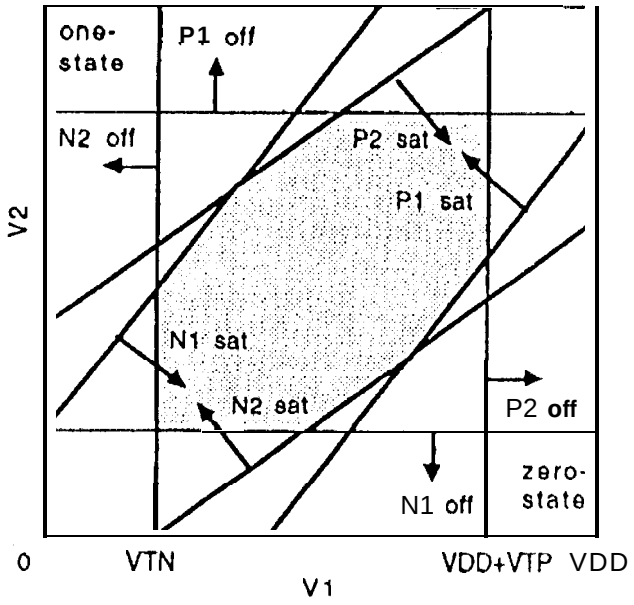

Fig. 6. *All four transistors are saturated in the* shadowed *area.* $\delta_n = \delta_p = 0.3$, $V_{TN} = -V_{TP} = 1$ v.

[1] This region is given by

$$\frac{V_1-V_{TN}}{1+\delta_n} \leq V_2 \leq V_{DD} + \frac{V_1-V_{DD}-V_{TP}}{1+\delta_p}$$
$$\frac{V_2-V_{TN}}{1+\delta_n} \leq V_1 \leq V_{DD} + \frac{V_2-V_{DD}-V_{TP}}{1+\delta_p}$$
$$V_{TN} \leq V_1 \leq V_{DD} - V_{TP}$$
$$V_{TN} \leq V_2 \leq V_{DD} - V_{TP}$$

The previously obtained straight line Solution for the case of $\beta_n=\beta_p$, given in Eq. (10), is simply a special case[2] of the general solution.

A plot of the dividing line for the case of β_n/β_p= 3.3 is shown in Fig. 7 using C_1/C_2 = 1, 0.7, 0.5, 0.25 and 0.1 as parameter values, As indicated by Fig. 7, the dividing line is very close to a straight line also for $\beta_n \neq \beta_p$[3]. As an example, the second order deviation in V2 for $V_1=V_{DD}$ is less than 5% for β_n/β_p=3.3 and $C_1/C_2 \geq 0.1$.

Comparisons to SPICE simulations show that the solution of Eq. (17) can be extended with small errors also into regions of the state-plane where one transistor is linear, if the current through this transistor is small compared to the current through the other transistor of the same inverter. For the example of Fig. 7, where β_n/β_p = 3.3, transistor P1 becomes linear along the dividing line when $C_1/C_2 \leq$ ().39. However, the error is negligible as long as i_{p1} is less than one tenth of i_{n1} (which is true for $C_1/C_2 \geq 0.07$).

For the limiting case of very small C_1/C_2 capacitance ratios, the dividing line becomes a horizontal line through the metastable state. The return track from the metastable state to one of the stable states coincides with the static transfer curve (i_1=0). For very large C_1/C_2 capacitance ratios the limiting dividing line is a vertical line through the metastable state. The return track from the metastable state to one of the stable states now coincides with the other static transfer curve (i_2=0). Sec Appendix,

[2] For $\beta_n=\beta_p$, Eq. (17) yields

$$C_2(V_{DD}+V_{TP}-V_{TN})(V_2-V_M)^2 = C_1(V_{DD}+V_{TP}-V_{TN})(V_1-V_M)^2,$$

from which Eq. (10) can be obtained. For that part of the dividing line that falls outside the shaded region where all four transistors are saturated, for instance when P2 is turned off (for $C_1/C_2<1$), Eq. (22) yields

$$C_1[(V_1-V_{TN})^3 - (V_{DD}+V_{TP}-V_M)^3 - (V_M-V_{TN})^3] = 3C_2(V_{DD}+V_{TP}-V_{TN})(V_2-V_M)^2,$$

which only slightly deviates from a straight line.

[3] It is exactly a straight line for $C_1=C_2$.

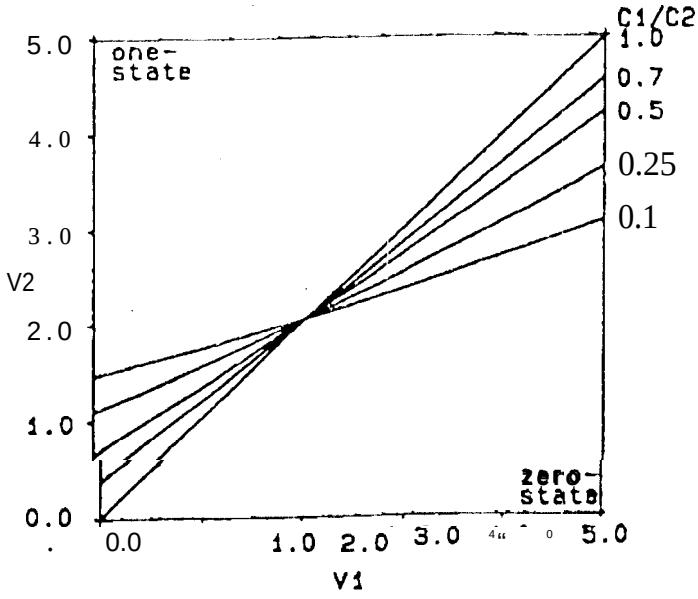

Fig. 7, The dividing line with C_1/C_2 = 1, 0,7, 0.S, 0.25 and 0.1 as parameter.

Critical Charge Expressions

To calculate the upset-rate of a static RAM in space, Buchler and Allen used the Petersen equation [7] which assumes a 10-percent worst case differential cosmic-ray spectrum. According to the Petersen equation, the upset rate (in upsets per bit-day) for a heavy-ion hit on a q-type reverse-biased pn-junction of node i is given by

$$R_i = 5\cdot10^{-10}\, AJ_{qi}\left(\frac{X_q}{QC_{qi}}\right)^2, \qquad (19)$$

where AJ_{qi} is the area of the reverse-biased pn-junction of node i (in μm^2), X_{qi} is the carrier collection depth of the same junction (in μm) and QC_{qi} is the critical charge (in pC).

The critical charge for a heavy-ion-induced up.set can be calculated for each reverse-biased pn-junction of the RAM cell using the results from the previous analysis.

For $C_1/C_2<1$, the critical charges for a hit of inverter 2 is calculated as follows. With the RAM cell being in the zero-state, V_2=0 and the drain of transistor P2 is reverse-biased. The critical voltage, VC_{p2}, for a P2 heavy-ion hit is obtained from the dividing line at $V_1=V_{DD}$ [1]. In the one-state, $V_2=V_{DD}$ and the drain of transistor N2 is reverse-biased. The critical

voltage, VC_{n2}, for an N2 heavy-ion hit is obtained from the dividing line at V_1=O [1].

Therefore, the critical voltages can be obtained from the straight line equation (10) as

$$VC_{p2} = V_M + \sqrt{\frac{C_1}{C_2}}\,(V_{DD} - V_M) \qquad (20)$$

and

$$VC_{n2} = V_M \sqrt{\frac{C_1}{C_2}}\,V_M, \qquad (21)$$

respectively.

The expression for VC_{p2} of Eq. (20) can be compared to the expression derived by Buehler and Allen. They based their analysis on the empirical observation that

$$\frac{dV_2}{dV_1} = \frac{V}{V_{DD}} \qquad (22)$$

at (V_{DD}, VC_{p2}) in the state-plane. After some approximations their derivation yielded

$$VC_{p2} = V_{TN} + \sqrt{\frac{C_1}{C_2}}\,(V_{DD} - V_{TN}). \qquad (23)$$

Here, it can be seen that while their expression for VC_{p2} only depends on the threshold voltage of the n-channel transistors, the new expression in Eq. (20) depends on the switching voltage of the inverter. Thereby, the influence of both the p- and n-channel transistors are considered,

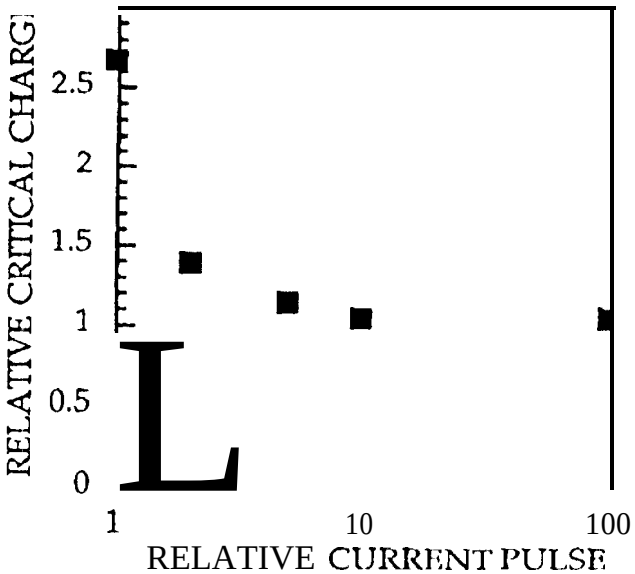

Fig. 8. The relative critical charge for memory upset versus the relative current pulse (normalized to the transistor saturation current).

From the critical voltages, VC_{p2} and VC_{n2}, Buehler and Allen [1] defined the corresponding critical charges for memory upset by a P2- and N2-hit as

$$QC_{p2} = C_2\,VC_{p2} \qquad (24)$$

and

$$QC_{n2} = C_2\,(V_{DD} - VC_{n2}), \qquad (25)$$

respectively.

The critical charge is the minimum charge needed for memory upset, assuming that the charge is collected so rapidly that the voltage on the other node does not change. This is true for most memory cells since they, typically, have a SIOW response time (>500 ps) and most of the charge is collected within 200 ps as shown by [4]. However, if charge is lost during the alpha hit and, more charge must be collected to upset the cell. To simulate the cell during the alpha hit, one must be concerned with the detailed nature of the current pulse. For 5 MeV alpha particles, the current pulse can be approximated by a decaying exponential with a time constant of 1 ns [3]. However, in most cases, as the simulated cases shown in Fig, 8, a simple square-wave current pulse is a good enough first-order approximation [8]. The corresponding set and release trajectories simulated for five-different current sources are shown in Fig. 9.

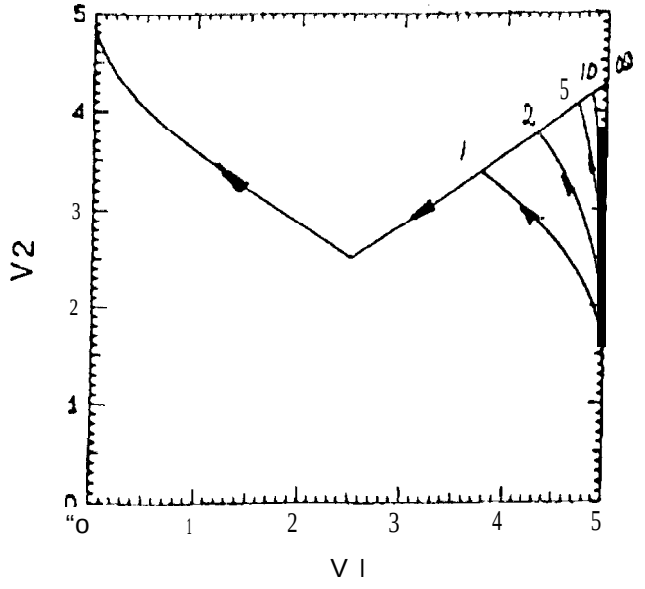

Fig. 9. The set and release trajectories for five different current pulses during the alpha hit. The current pulse is normalized to the transistor saturation current.

The critical charges for a hit of inverter 1 can be calculated similarly. at least for capacitively symmetric RAM cells or when $C_1/C_2>1$. In order to estimate the critical charges for N1 or P1 hits when $C_1/C_2<1$, one has to know how the dividing line continues into the regions where $V_1<0$ and $V_1>V_{DD}$. Due to the forward biasing of the drain diodes N1 or P1, respectively, large restoring currents i_i develop, bending the dividing line almost horizontal outside the frame of Fig. 7. Consequently, the dividing line will be impossible to reach by N1 or P1 hits, i. e. QC_{N1} and QCp_i become very large and the corresponding upset rates can be neglected.

Conclusions

A dynamic description of the charging and discharging behavior of bistable RAM cells after single event upsets has been developed. State plane analysis has been shown 'to be a useful tool in providing insight into basic RAM ccl] behavior, both in the set mode during alpha particle hit and in the release mode, after the hit. The state plane has been shown to be divided into two halves by a dividing line that determines to which stable state the system returns after a hit. Analytic expressions for the dividing line, and for the minimum critical upset charges, have been given.

Acknowledgements

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References

1. **M.** Buehler and R. Allen, "An Analytical Method for Predicting CMOS SRAM Upsets with Application to Asymmetrical Memory Cells", *IEEE Transaction on Nuclear Science,* NS-33, pp 1637-1641 (19$36)
2. R. C. Jaeger and R. M, Fox, "Analytic Expressions for the Critical Charge in CMOS Static RAM Cells", *IEEE Transactions on Nuclear Science,* NS-30, *4616-4619* (1983)
3. R. J. McPartland, "Circuit Simulations of Alphtr-Particle-Induced Soft Errors in MOS Dynamic RAM 's", *IEEE Journal of Solid-State Circuits, SC-16,31-34 (1981)*
4. C. M. Hsieh, P. C. Murley and R. R. O'Brien, "Dynamics of Charge Collection from Alpha-Particle Tracks in Integrated Circuits", in *Proceedings of 10th Annual International Reliability Symposium,* Orlando, FL, 38-42 (1981)
5. L. A. Glasser and D. W. Dobberpuhl, *The Design and Analysis of VLSI Circuits,* Chap 5 (Fig.5.38), Reading, MA, USA: Addison-Wesley, (1985)
6. D. K. Arrowsmith and C. M. Place, *Ordinary Differential Equations,* London, New York: Chapman and Hall (1982)
7. E. L. Petersen, J, B. Langworthy and S. E. Diehl, "Suggested Single Event Upset Figure of Merit", *IEEE Transaction on Nuclear Science,* NS-30, pp 4533-4539 (1983)
8. Y. Idei, N. Homma, H. Nambu and Y. Sakurai, "Soft-Error Characteristics in Bipolar Memory Cells with Small Critical Charge", *IEEE Transactions on Electron Devices, ED-38, 2465-2471 (1991)*

Appendix

Generally, Eqs (1) and *(2)* can be rewritten as

$$\frac{dV_1}{dt} = \frac{i_1}{C_{11}} + \frac{i_2}{C_{12}} \tag{A1}$$

$$\frac{dV_2}{dt} = \frac{i_1}{C_{21}} + \frac{i_2}{C_{22}} \tag{A2}$$

where

$$C_{11} = C_1 + \frac{C_m}{1 + \frac{C_m}{C_2}} \tag{A3}$$

$$C_{12} = C_2 \frac{C^*}{C_m} + C_1 + C_2 \tag{A4}$$

$$C_{21} = C_1 \frac{C_2}{C_m} + C_1 + C_2 \tag{A5}$$

$$C_{22} = C_2 + \frac{C_m}{1 + \frac{C_m}{C_1}} \tag{A6}$$

Using the following linear approximation of the transistor currents, .

$$i_1 = g_m (V_2 - V_M) + g_o (V_1 - V_M) \tag{A7}$$

$$i_2 = g_m (V_1 - V_M) + g_o (V_2 - V_M), \tag{A8}$$

where $g_m = g_{mn} + g_{mp}$ is the sum of the n- and p-channel transconductances in the metastable point (V_M, V_M) and go = g_{on} -t- g_{op} is the sum of the output conductance, wc obtain

$$\frac{dV_2}{dV_1} = \frac{a_2(V_2 - V_M) + b_2(V_1 - V_M)}{a_1(V_2 - V_M) + b_1(V_1 - V_M)}. \tag{A9}$$

Here

$$a_1 = \frac{g_m}{C_{11}} + \frac{g_o}{C_{12}}, \qquad a_2 = \frac{g_m}{C_{21}} + \frac{g_o}{C_{22}}, \tag{A10}$$

$$b_1 = \frac{g_o}{C_{11}} + \frac{g_m}{C_{12}}, \qquad b_2 = \frac{g_o}{C_{21}} + \frac{g_m}{C_{22}}. \tag{A11}$$

Assuming a linear relationship between V_2 and V_1 along the dividing line, i. e.

$$V_2 - V_M = K (V_1 - V_M), \tag{A12}$$

we obtain the slope

$$K = -\frac{1}{2}\left(\frac{b_1}{a_1} - \frac{a_2}{a_1}\right) \pm \sqrt{\frac{1}{4}\left(\frac{b_1}{a_1} - \frac{a_2}{a_1}\right)^2 + \frac{b_2}{a_1}} \tag{A13}$$

If the mutual capacitance can be neglected compared to the load capacitances, the expression for the slope reduces to

$$K = \pm\sqrt{\frac{C_1}{C_2} + c^2} - c \tag{A14}$$

where

$$c = \frac{1}{2}\frac{g_o}{g_m}\left(1 - \frac{C_1}{C_2}\right).$$

As expected, this expression reduces further to $K = \pm\sqrt{\frac{C_1}{C_2}}$ when assuming $g_o = 0$. Assuming $g_o \neq 0$ and letting $C_2 \to \infty$, we obtain from Eq. (A14)

$$K = \begin{cases} 0 \\ -\dfrac{g_o}{g_m} \end{cases}, \tag{A15}$$

which confirms an incoming horizontal line to the metastable state and an outgoing line with a slope given by the reciprocal gain of the inverter. Letting $C_1 \to \infty$, we obtain

$$K = \begin{cases} \infty \\ -\dfrac{g_m}{g_o} \end{cases}, \tag{A16}$$

which confirms an incoming vertical line to the metastable state and an outgoing line with a slope given by the gain of the inverter.

Finally, if the mutual capacitance cannot be neglected, we obtain assuming $g_o = 0$

$$K = \pm\sqrt{\frac{C_{11}}{C_{22}}}. \tag{A17}$$